MINIATURISATION OF A BAND-X MONOLITHIC GaAs AMPLIFIER

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Abstract

Reducing the area occupied by microwave monolithic integrated circuits is a necessity to decrease the cost of these circuits. A reduction in area can be obtained with circuit configurations comprising a minimum of inductances and by using spiral inductors. When a circuit is compacted, the coupling between radiating elements such as the inductances has also to be taken into account. An amplifier working from 2 to 10GHz with a measured gain of 5.8 ± 0.4dB is presented. The efforts to reduce the area have led to a surface of $0.16mm^2$ and therefore an integration density of $36dB/mm^2$.

1.Introduction

Evolving from the design techniques of hybrid microelectronics, the design of monolithic microwave integrated circuits (MMIC) on GaAs does not necessarily make maximum use of the available surface area. Because of this, the area occupied by MMIC is very large in comparison with the surface occupied by logic circuits on GaAs. A study of some recent circuits shows that about 40% of the surface is taken up by inductances or transmission lines, 20% by ground electrodes, 10% by capacitors, 5% by transistors and 25% by wasted space. The larger the area of a circuit, the higher its cost and for systems involving large numbers of chips such as phased array antennae, the cost aspect becomes relevant to the feasability of the whole project. Reducing the area of a circuit (or increasing the integration density) is therefore a most important aspect of study for monolithic circuit designs.

The aim of the work presented here is to fabricate an amplifier with a single stage, having a bandwidth of 2 to 10GHz and occupying an area of GaAs as small as possible. The design and fabrication of a compact circuit are shown and compared with a circuit previously fabricated along more classical lines. We also describe the design of a compact circuit with an on-chip active biasing circuitry.

2.Design of the circuit

From the distribution of area usage mentioned above, it is obvious that an important decrease in circuit dimensions can be obtained by reducing the number of inductances and lines as well as the amount of unused spaces.

Taking into account the first point leads to a configuration with only one inductance in the input and one inductance in the output circuits. This circuit (Fig.1) which consists effectively of low pass filters, allows not only external biasing arrangements, but also on-chip active biasing.

In order to reduce the unused space, the inductances have been designed with spiral inductors and the various circuit elements have been condensed more closely together. The resultant increased coupling is accounted for and accommodated into the circuit design.

A model for the spiral inductor was obtained using the equivalent circuit shown in figure 2. In this diagram, the values of the inductances are obtained from a computation taking into account the mutual inductance between each turn.

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The capacitances between turns ans with respect to the back face ground plane are given by a numerical programme that computes the microstrip lines characteristics using Green functions (1). Coupling between input and output inductors was calculated by using the simplified diagram of figure 3 and a circuit simulation programme which takes into account the coupling between multiconductors such as that of branches 1,2,6 and 8 of figure 3. The results of this computation give a coupling of - 44dB at 10GHz when the propagation occurs in the directions indicated in the figure and a coupling of - 35dB when one of the directions of propagation is changed.

The transistor geometry has been changed, reducing its area by a factor of 3.
Typical values of the elements of the equivalent circuit of the FET are :

C_{gs} = 0.33pF
Go = 30mS
Ro = 350 Ω
C_{DS} = 40 fF
R_g+Rc = 15Ω

Fig.4 shows the simulated response of $|S_{21}|$ for the final design. Capacitors C_2 and C_3 of figure 1 are no longer necessary.

An analysis of the variations of the gain as a function of tolerances of the elements of the circuit has been performed. Figure 4 shows a worst-case analysis when only the passive elements and only the active elements are varied of $\pm$ 10%. For passive element, the correlated values such as the ε of SiO_2 for capacitances or the ε_{eff} of the lines are varied at the same time. For the transistor, each element of the equivalent circuit was varied in an uncorrelated way giving a result which must be interpreted with a minimum of precaution. Nevertheless, the results show the greater sensitivity of the response to the variation of the physical values of the transistor. A stability analysis shows an unconditional stability from 3 to 12GHz and a good stability with a load of 50Ω for lower frequencies.

3.Fabrication and measurements

The circuit was fabricated on a VPE layer with an active layer concentration of $1 \times 10^{17} cm^{-3}$ and the FET has a total gate width of 260µ with 0.7µ gate length.Electron beam lithography is used throughout. The dielectric used for the matching circuit capacitors and the crossovers in the spiral inductor is SiO_2. To improve the acuracy of the capacitor values and to reduce edge breakdown a special double thickness technique is used. A thin layer of dielectric is deposited to make the capacitor itself and then a second layer is deposited on the edges of the capacitors (Fig.5). This second layer can also be used to decrease the capacitance at the crossover of two lines.

Triangle points of figure 4 show the measurement results for the $|S_{21}|$ and figure 6 shows a comparison between measurements and simulation for S_{11} and S_{22}. The measured gain is 5.8 $\pm$ 0.40dB for a FET current of 64mA. For a current of 20mA, the gain is 5.2 $\pm$ 0.8dB and the noise figure is less than 5.4dB.

The dimensions of this amplifier(including bonding pads)are 775 x 210µ giving an area of $0.16mm^2$. Figure 7 shows a comparison in area with another amplifier realised following a more classical design (2) and having a gain of 7dB at 10GHz. The dimensions of the preceding amplifier are 1850 x 800µ corresponding to an area of $1.5mm^2$. Between these two amplifiers, the difference in area is about a factor of 10.

4.Design of an amplifier with on-chip biasing

A second design including an on-chip biasing circuit has been launched. The biasing circuit consists of two active loads and decoupling capacitors C_1, C_2 and C_3 as shown on figure 8. In these capacitors the dielectric is made of a layer of Ta_2O_5 which increases the area of the circuit only by 40%. The mask of this circuit is presented on figure 9.

5.Conclusion

A single stage amplifier working from 2 to 10GHz with a gain of about 6dB has been designed and fabricated within an area of 0.16mm^2. These results concern an amplifier design using external biasing facilities, however a subsequent version has been designed in which active bias and decoupling circuity is included on the same chip for an increase of only 40% in the area.

Bibliography

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Proceedings of the 11th European Microwave Conference, Amsterdam, 1981.

2-C.Rumelhard, P.Duême, P.R.Jay, M.Le Brun
"Miniaturisation des amplificateurs monolithiques sur AsGa à 10GHz"
Revue Technique THOMSON-CSF, vol 15, no 1, March 83, p. 183

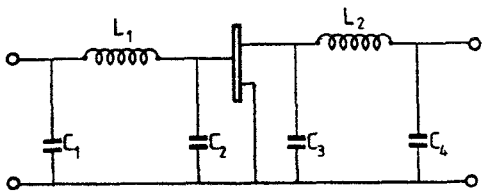
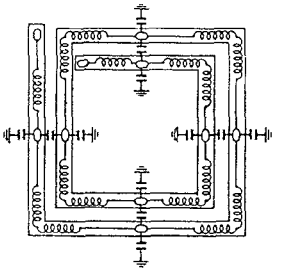


Figure 1 : *Amplifier diagram*



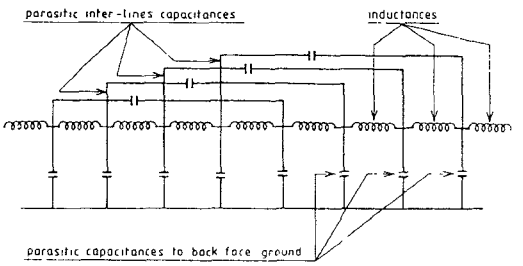


Figure 2 : *Spiral inductor modelisation*

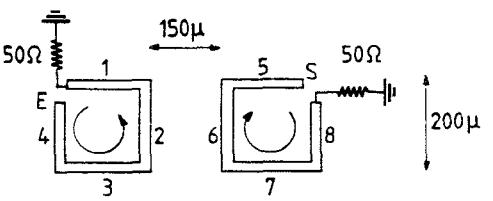


Figure 3 : *Coupling between spiral inductors*

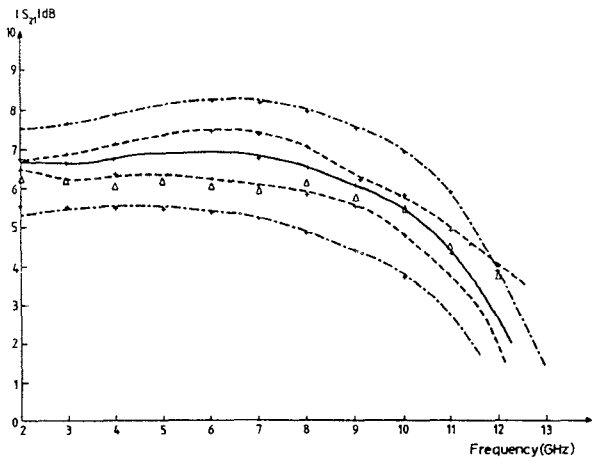


Figure 4 : *Gain versus frequency*

——— : *nominal gain*

------ : *worst case analysis for ± 10% variation on passive elements*

-.-.-. : *worst case analysis for ± 10% variation on values in the transistor equivalent circuit*

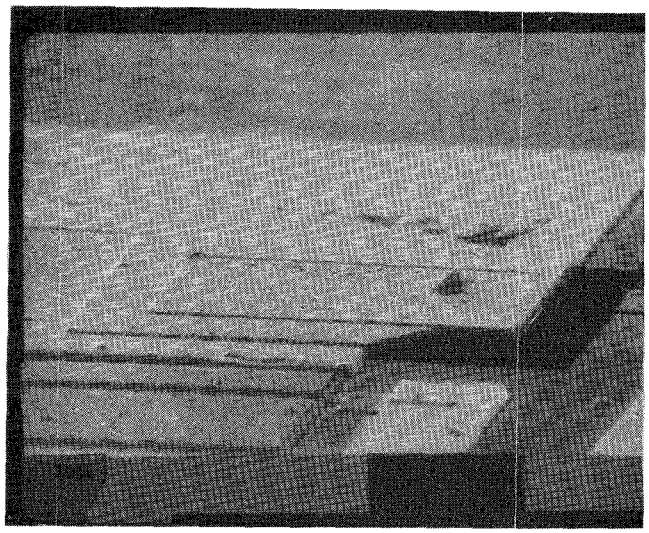


Figure 5 : Photograph of a capacitor

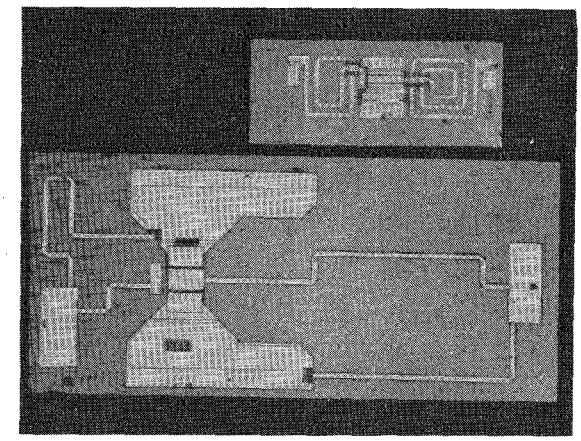


Figure 7 : A classical design and the effect of the miniaturisation

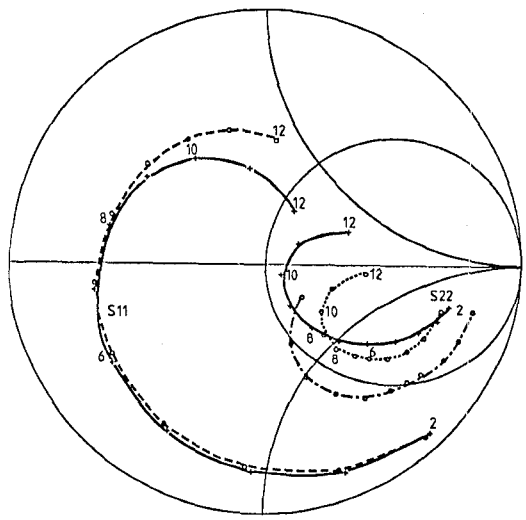


Figure 6 : Reflection coefficients

——— : calculated

------ : measured (V_D = 3 V)

-.-.-. : measured (V_D = 4 V)

(Frequency is in GHz)

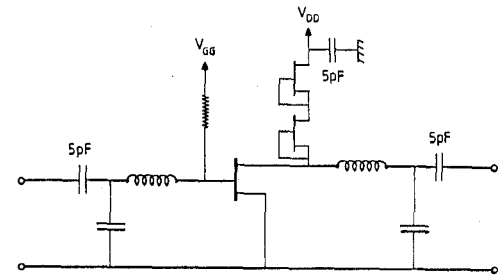


Figure 8 : On-chip biasing circuitry

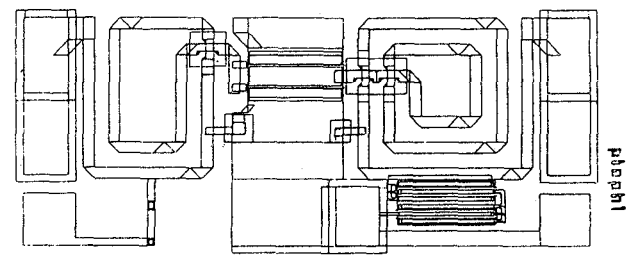


Figure 9 : Mask of the amplifier with on-chip biasing